REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-3, 5-17 and 21-25 have been canceled. Claims 26-43 are newly added. No new matter has been added.

Petition to Revive

Accompanying this Amendment and Response is a Petition to Revive under 37 CFR § 1.137(b) and Declarations of Motoaki Saito and James A. Finder supporting said Petition.

Changes to Specification

Various amendments have been made to the specification to correct typographical errors and other minor matters of form.

Regarding the changes to page 5 of the Substitute Specification, which start at line 10, Applicant wants to emphasize that no new matter has been added. The language added to page 5 regarding the bus structure is inherently supported in the original specification, as filed, particularly in Figure 3. In addition, that subject matter is also described in the annex ("IMAGINE: The Image Engine -- Documentation & User's Manual") that was included as part of the original filing of this application and which is incorporated into the specification by reference (at Substitute Specification, page 9, lines 21 et seq.). See, for example, the annex at page 21, last paragraph of the right column, and page 25, second paragraph of the left column.

Response to Rejections

Claims 1-3, 5-17 and 21-25 were rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,465,224 of Guttag et al. ("Guttag"). Claims 1-3, 7-17 and 21 were also rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 4,901,267 of Birman et al. ("Birman") in view of U.S. Patent No. 4,953,119 of Wong

et al. ("Wong") and U.S. Patent No. 4, 418, 383 of Doyle et al. ("Doyle") and further in view of Guttag.

The previously pending claims have been replaced by new claims 26-43. The cited references neither disclose nor suggest, either individually or in combination, the as an invention as defined in claims 26-43.

Independent claim 26, for example, recites:

> 26. (New) A processor comprising:
> a plurality of functional units;
> a bus structure including *a plurality of buses, including a bus for each of the functional units*; and
> *a plurality of bus registers, each coupled to an output of only a corresponding one of the plurality of functional units and to only a corresponding one of the plurality of buses.*
> (Emphasis added.)

None of the cited references discloses or suggests a processor that includes a plurality of buses including a bus for each of a plurality of functional units, and a plurality of bus registers, wherein each bus register is coupled to an output of only a corresponding one of the plurality of functional units and to only a corresponding one of the plurality of buses. In other words, in the present invention, each of the plurality of functional units has a dedicated bus register and a separate bus coupled to the output of the corresponding bus register.

This structure allows for extremely fast and efficient communication of data between the functional units in the processor. This technique is, therefore, particularly advantageous in the field of graphics processing. In certain embodiments, the dedicated bus registers and buses can be explicitly referenced in the assembly code, such that the assembly code defines the routing from one functional unit to another with the help of the bus registers.

The cited references neither disclose nor suggest the above-noted claim features. Consequently, independent claim 26 and all claims which depend on it are patentably

distinguishable from the cited art. The other independent claims include similar limitations to those discussed above, as well as additional limitations, and are therefore patentable for similar reasons, at least.

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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Date: 8/20/02

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August 20 2002
(Date of Deposit)

Julie Arango
(Typed or printed name of person mailing correspondence)

Julie Arango 8/20/02
(Signature of person mailing correspondence)

MARKED-UP VERSION SHOWING CHANGES

IN THE SPECIFICATION:

Please amend the specification as follows (referring to pages and lines of the Substitute Specification filed on Oct. 14, 1999):

Replace the paragraph beginning at page 2, line 26 with the following paragraph:

- a register unit provided with at least two registers for storing the integer data words of eight bits or multiples of a bits on which the operation and/or pipeline multiplication has to be [perfor5 mea] performed; and

Replace the paragraph beginning at page 3, line 17 with the following paragraph:

Further advantages, features and details of the present invention will be elucidated on the basis of the following description of a preferred embodiment thereof with reference to the annexed [drawing] drawings, in which: [fig. 1 shows a functional diagram of a graphic application of the data processing circuit according to the present invention;]

Fig. 1 is a functional diagram of a graphic application of the data processing circuit according to the present invention;

Replace the paragraph beginning at page 5, line 10 with the following paragraph:

[ ]The bus structure 26 (Fig. 3) comprises a control SC-bus 51, an A-bus [S2] 52, a B-bus 53, a Q-bus 54, an F -bus [5S] 55, an M-bus 56, a U-bus 57, a D-bus 58 and a V-bus 59, each of which [are] is, for instance, 32 bits wide. Each of several functional

units of data processing circuit 1 drives its own output bus and has a separate, dedicated output (bus) register/driver for its bus, which can be read in the following cycle by various other functional units. For example, multiplier 23 drives the M-bus 56 using its bus register, M-reg 66; ALU 31 drives the F-bus 55 using its bus register, F-reg 64; shift register 25 drives the Q-bus 54 using its bus register, Q-reg 62; register bank 33 drives the A-bus 52 and B-bus using bus registers, A-reg 60 and B-reg 61, respectively; image input and output circuitry 30 drives the V-bus using its bus register, V-reg; and so forth. This approach allows parallel processing for all of the functional units.

Replace the paragraph beginning at page 5, line 16 with the following paragraph:

The register bank 33 is connected via output registers 60 and 61 to the [A and B bus] A-bus and B-bus, respectively. A register bank 33 contains [ninty-six] ninety-six inputs which are single 32 bit, double 16 bit or quadruple 8 bit words. Three ports enable simultaneous performance of two read actions and a write action. Sixty-two of the [nenty-six] ninety-six registers are directly accessible. The remaining thirty-two inputs are addressed via the vector index generator 32 which can generate a maximum of 12 locations per cycle (i.e., four byte sections for each of the three ports, since each word segment can be selected separately within the registers).

Replace the paragraph beginning at page 5, line 21 with the following paragraph:

The parallel shift register 25 is designed such that it can shift 32 bits of data anywhere from 1 to 32 positions to the left or right in one clock cycle based on the information received via the A-bus 52. The information can be grouped into one, two or four sections of 32, 16 and 8 bits respectively. The shift can take place logically (unsigned), numerically (unsigned) and rotatingly. The operations are received from the B-bus 54 or the F-bus [S5] 55. The parallel shift register 25 is connected via a register 62 to the Q-bus [s4] 54. Fig. 8 schematically shows an example of the two step rotation

of a 32 bit word (consisting of two 16-bit bytes) through 11 bits in a positive direction by way of four 8 bit rotations and eight 4 bit crossings.

Replace the paragraph beginning at page 6, line 2 with the following paragraph:

With reference to Fig. 3, the arithmetic logic unit 31 (ALU) is connected to the A-bus [S2] 52, the Q-bus 54, the M-bus 56, the D-bus 58, the U-bus 57, the B-bus 53, the F-bus 55, again to the U-bus 57 and the V-bus 59. All the usual logic operations of a conventional ALU can be performed by the ALU 31 of the present invention in addition to numerical functions such as addition, subtraction, increment and decrement. The ALU 31 is further provided with a so-called parametric logic function. On the basis of the content of an 8 bit register, the ALU 31 can perform a random combination of 256 possible logic operations on 3 operands. The standards for X-window and MS-Windows specify that logic and graphic operations must be possible in any combination. The parametric function can also be used to realize shifting, masking, combining or comparing operations in a single clock cycle.

Replace the paragraph beginning at page 8, line 10 with the following paragraph:

The drive of the image memory 29 is adapted to generate an address on the basis of the X/Y position so that any random image segment can be addressed on the basis of its location and the image [and] in the image [memo- ry] memory. The image memory is also suitable for storing other databanks such as lists and databanks with graphic elements.

Replace the paragraph beginning at page 8, line 13 with the following paragraph:

The data processing circuit [can] 1 can be programmed in a higher program language, such as C, so that it is easily programmed, as in RISC and CISC processing units. The data processing circuit 1 can be programmed with instructions according to the RISC concept as well as with the CISC instructions of a personal computer. In order to achieve a large increase in speed for graphic applications, the programmer can program all functions of data processing circuit 1 at a lower-level via an instruction field of 64-bits. The ALU 31 and the multiplier unit can be set to parallel operations, whereby the speed for graphic applications can be increased by a factor of 4-20 as compared to existing RISC processors. For a particular application, a programmer will set a "once-only" series of instructions and control registers. Subsequently the programmer will start the processor with one command, ["]hereafter the processor independently processes the pixel flows.

Replace the paragraph beginning at page 9, line 21 with the following paragraph:

[Since it is practically impossible to describe all the possibilities of the present invention on account of its complexity, a] A product specification entitled "IMAGINE: The Image Engine -- Documentation & User's Manual" (version 2.80), provides additional details of embodiments of the data processing circuit 1 and is incorporated herein by reference[, insofar as this is completed,] and is appended as an annex to this specification. [As is usual in this technical field the specification is written in the English language. After completion it will become part of the public domain, probably within a year.]